A 12-dB High-Gain Monolithic Distributed Amplifier

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Abstract—**By reducing gate and drain line loss associated with the active elements of a distributed amplifier, significant gain improvements are possible. Loss reduction is achieved in a novel monolithic distributed amplifier by replacing the common-source FET's of the conventional design with cascode elements having a gate length of one-quarter micron. A record gain of over 10 dB from 2 to 18 GHz and a noise figure of 4 dB at 7 GHz have been achieved on a working amplifier. Details of the design and fabrication process are described.**

I. Introduction

BY ABSORBING parasitic FET capacitance into artificial transmission lines, distributed amplifiers offer extremely broad band performance capability. However, such amplifiers have been characterized by relatively low gain. R. Pauly *et al.* [1] have reported a 2–40-GHz amplifier with 4-dB gain and a 9-dB noise figure. Other workers have reported designs achieving about 7 dB in the 2–20-GHz range [2]. A high-gain distributed amplifier would have several performance advantages in practical applications, such as a broad-band 20-dB gain module. A reduction in the required number of stages and subsequent current consumption, interstage loss, and gain ripple would be feasible.

A detailed analysis of the conventional common-source FET distributed amplifier [3] shows that the bandwidth of the amplifier is limited by the gate capacitance of the FET. Also, the gain is limited by loss associated with the gate and drain line loading by the FET's. For an amplifier utilizing common-source FET's, the gate and drain line signals are dissipated by internal resistance within the FET, as well as external source inductance. The dissipation increases with frequency; in fact, our studies indicate that the input signal is nearly absorbed by the gate line at the upper bandedge in a properly designed amplifier. If these loss mechanisms are somehow mitigated, particularly at the higher frequencies, the gate and drain lines can accommodate additional gate periphery, and the gain–bandwidth product increases. From the standpoint of designing the perfect distributed amplifier, then, the ideal active element is one with infinite input and output impedance as well as infinite voltage gain. Clearly, the common-source FET does not meet these requirements; in fact, a modified active element composed of one or more FET's and passive elements may be more suitable.

Manuscript received May 5, 1986; revised July 28, 1986.

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IEEE Log Number 8611161.

This paper reports the use of quarter-micron-gate-length FET's in a cascode circuit configuration as an alternative to the longer gate length common-source FET for broadband distributed amplifiers. A novel 2–20-GHz distributed amplifier has been designed for a gain of 12 dB $\pm$ 0.25 dB. Gain exceeding 10 dB from 2 to 18 GHz and a minimum noise figure of 4 dB at 7 GHz have been achieved on working circuits. The cascode circuit configuration is modeled using a single-gate FET model. Ease of modeling as well as fabrication dictated the use of cascode elements over dual-gate FET's. Other features which facilitated the high-gain result include a variable parameter circuit design in which FET widths and inductive stub lengths were optimized for best performance. Additionally, the amplifiers were fabricated on OMVPE material with uniformly doped active layers. Uniform doping permits a deeper gate recess and reduced I_{dss} without degradation of FET performance. Thus, low noise figure and high associated gain are compatible; in fact, the 4-dB noise figure reported had an associated gain of 10 dB. Details of all the aforementioned features are described in the following sections.

II. The Cascode Element

As mentioned previously, the ideal active element for a distributed amplifier is one with infinite input, output impedance and infinite voltage gain. Some attempts have been made to modify or replace the conventional half-micron-gate-length, common-source FET with a device that exhibits superior input and output characteristics.

A remedy that has been used to reduce gate-line loading and extend bandwidth is to use shorter gate length FET's with their reduced gate capacitance [1]. The input impedance of the common-source FET is approximately

$$Z_{\text{in}} = r_i + \frac{1}{j\omega C_{gs}}. \tag{1}$$

An empirical expression for r_i based on equivalent circuit modeling of both quarter-micron and half-micron FET's fabricated in the lab is

$$r_i = \frac{1}{2g_m}. \tag{2}$$

For instance, this relationship holds for the FET model in Fig. 3. Reducing the gate length reduces C_{gs} and may increase g_m. Thus, Z_{in} is more reactive, loss is reduced, and bandwidth is extended. However, short-gate-length

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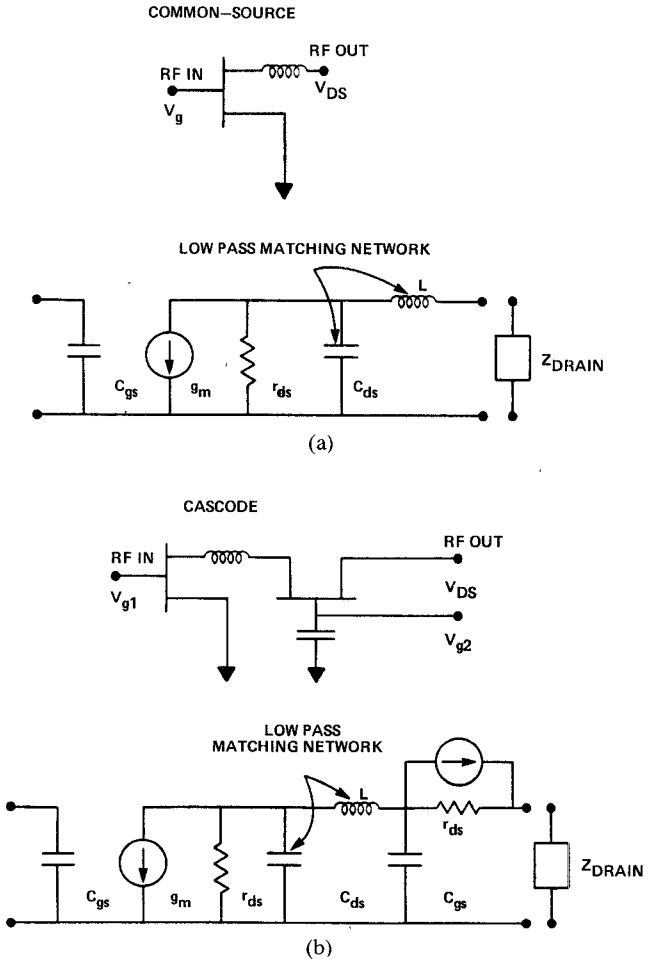

Fig. 1. (a) Common-source element and approximate small-signal model used in conventional amplifier design. (b) Cascode element with biasing and approximate small-single model. Both elements incorporate a partial matching L section.

FET's can exhibit increased output conductance [4], which can thwart significant improvement in gain. Our own calculations show that little gain improvement, beyond the 7-dB gain of longer gate length circuits, is achievable.

A remedy that has been used to reduce output conductance is to use the two-FET cascode active element. D. Dawson *et al.* [5] have demonstrated moderate gain improvements using one-micron-gate-length cascode sections in a 2–6-GHz hybrid distributed amplifier. Referring to the small-signal equivalent circuit of Fig. 1(b), the dc output impedance of the cascode element is

$$Z_{\text{out}} = (\mu + 2) r_{ds} \tag{3}$$

where

$$\mu = g_m r_{ds} \approx 10. \tag{4}$$

Thus, the output conductance is reduced by a factor of ten, and this effect persists to high frequencies, as shown in Fig. 2.

The previous statements regarding the reduction of gate and drain parasitic loss can best be summarized using the S-parameter representation of the active element. It is useful to note that as the loss mechanisms of the active device increase, $|S_{11}|$ and $|S_{22}|$ both decrease. Thus, these

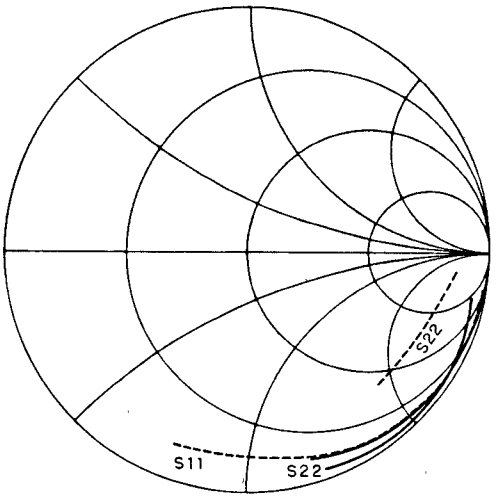

Fig. 2. $|S_{11}|$, $|S_{22}|$ for a common-source FET and a cascode active element. The cascode element has less loss, which is ideal for distributed amplifiers. --- common-source FET (0.5 μm, $N_d = 3.5\times10^{17}/\text{cm}^3$). —— cascode active pair (0.25 μm, $N_d = 5\times10^{17}/\text{cm}^3$).

two parameters serve as a good comparative measure of the usefulness of an active element for distributed amplifiers. In particular, Fig. 2 shows S_{11} and S_{22} for a half-micron-gate-length, common-source FET and a quarter-micron cascode active element. Note that over the entire bandwidth, $|S_{11}|$ and $|S_{22}|$ are closer to unity for the quarter-micron cascode device.

Further insight is gained into the cascode operation by comparing it with its common-source predecessor in Fig. 1. The cascode element is similar to the common-source device, except for the series-connected common-gate FET. In both cases, however, an L-section composed of drain–source capacitance C_{ds} and high-impedance stub of inductance L provides a high-frequency matching section between the common-source FET and its corresponding load [6]. Peaking of the voltage gain is required to offset the loss due to the gate and drain lines, which is particularly acute at the upper bandedge of operation. For the common-source device, the L-section helps match the FET directly to the drain line. For the cascode element, matching occurs to the common-gate FET. The peaking behavior of the inductive stubs in both cases is quite similar. The fact that the voltage gain is similar for both devices is easily verified at dc by referring to Fig. 1. For the common-source device,

$$Av = g_m \frac{r_{ds} Z_{\text{drain}}}{r_{ds} + Z_{\text{drain}}} \approx g_m Z_{\text{drain}}. \tag{5}$$

For the cascode element

$$Av = \frac{\mu(\mu+1) Z_{\text{drain}}}{(\mu+2) r_{ds} + Z_{\text{drain}}} \approx \left(\frac{\mu+1}{\mu+2}\right) g_m Z_{\text{drain}} \approx g_m Z_{\text{drain}}. \tag{6}$$

In both cases, Z_{drain} at dc is assumed negligible compared to r_{ds}

$$Z_{\text{drain}} = 25\ \Omega \ll r_{ds}. \tag{7}$$

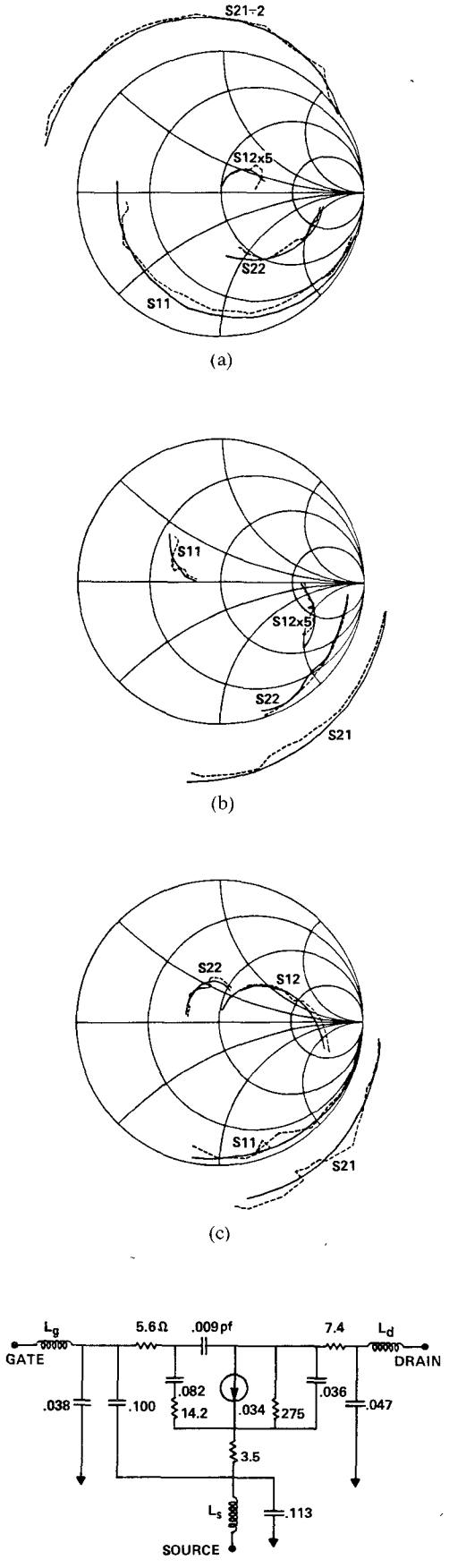

Fig. 3. Experimental and modeled S-parameters for a 0.25-μm×150-μm FET in the common-source (a), common-gate (b), and common-drain (c) configurations (——— model; ---- data). A single FET model was used to fit all three S-parameter data sets.

III. FET Modeling

Because the cascode active element is composed of a common-source FET in series with a common-gate FET, as shown in Fig. 1(b), reliable optimization of amplifier design parameters requires accurate modeling of devices in both configurations. The usual approach to FET modeling is to fit, via optimization algorithms, an equivalent circuit model to common-source S-parameter data alone. However, parasitics, innocuous in the common-source configuration and thus difficult to identify quantitatively, can dominate in the common-gate configuration. For instance, parasitic source–pad capacitance, essentially invisible in the common-source configuration, can have great influence in the common-gate configuration. A novel approach to FET modeling achieves the required accuracy by optimizing a single FET model to fit common-source gate and drain data for a single device. This new procedure results in a highly accurate FET model that can be utilized in any configuration. Fig. 3 summarizes the results of this procedure. A single 0.25-μm×150-μm FET was rebonded and remeasured in the three configurations. Note that the single optimized FET model in the lower left corner fits the data excellently.

IV. Circuit Optimization

Calculation of the cascode distributed amplifier design parameters required CAD optimization of 25 independent variables, including 12 gate and drain line lengths, five inductive stubs, and five FET widths. An extremely useful feature of our FET model allows for continuous variation of gate width during optimization. This is simply achieved by scaling the essential equivalent circuit elements, such as transconductance, with the width of the device. The two FET's composing each cascode element were constrained to have the same width. In order to ensure that a global optimum was achieved with such a prohibitive number of independent parameters, a sequence of optimizations was carried out in which increasing numbers of parameters were admitted to the optimization process. A preliminary optimization was carried out for a constant-K, constant-FET-width design. The last optimization included all 25 parameters. Compared to the constant-K design, the variable design has improved return loss, gain flatness, and 1–2 dB more gain. Recent experimental evidence for a similar common-source amplifier [7] has shown this to be the case.

The layout of the fabricated amplifier is shown in the photomicrograph of Fig. 4. Detail of the cascode element is shown in Fig. 5. The first two FET's separated by the longest inductive stub, near the input of the circuit, compose the first cascode element and are each 90 μm wide. The second to last cascode element, near the output of the circuit, is 250 μm wide. A qualitative understanding of the enhanced performance of the variable design compared to the constant-K design is possible. An optimized constant-K design has FET's of the same width and of the same length. By increasing the peaking for the first few cascode elements, high-frequency gain will rise. At high frequen-

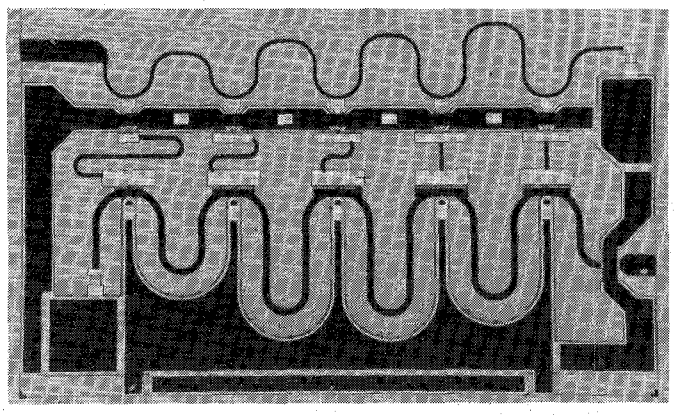

Fig. 4. A photomicrograph of the fabricated cascode distributed amplifier. Chip size is 1.8 mm × 3.0 mm. Common-gate bias is applied to the left or right tab or to the bottom edge of the chip. The gate line is near the top edge of the chip. Backside vias ground the chip at points indicated by the small white rectangles.

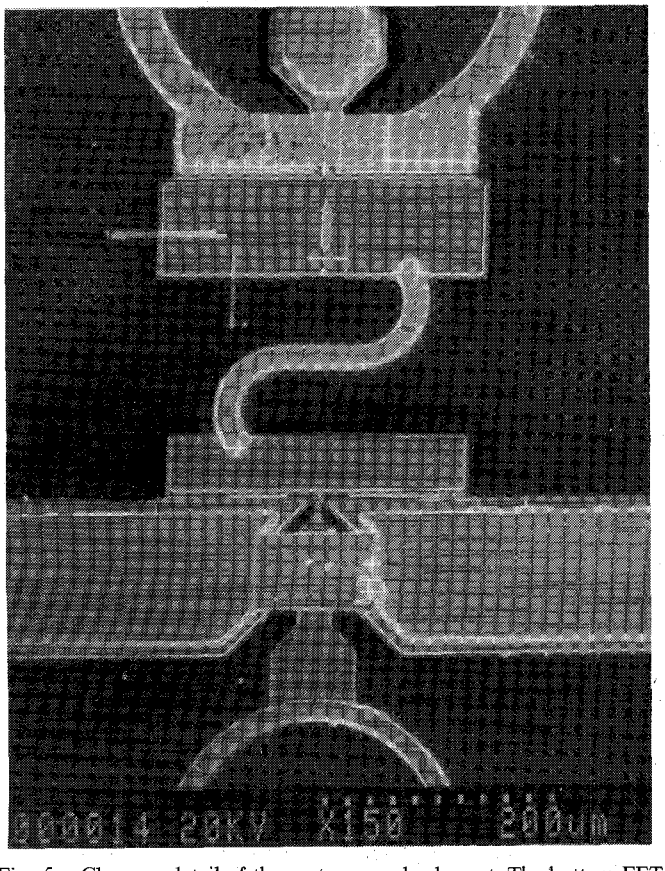

Fig. 5. Close-up detail of the center cascode element. The bottom FET is common-source and the top is common-gate.

cies, the input signal dissipates by the time it reaches the last cascode elements of the circuit. A good way to boost the low-frequency gain is to then increase the width of these FET's. Gain flatness is then restored, but at a higher gain level. This trend is clearly seen in the variable design shown in Fig. 4.

Final results of the optimization process are shown in Fig. 6 along with optimized results for less complicated circuits for comparison. Gain of 12 dB ± 0.25 dB from 2 to 20 GHz can be achieved for a distributed amplifier with

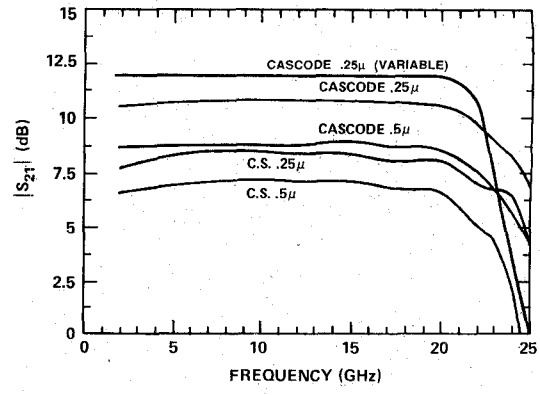

Fig. 6. A variety of optimized amplifier gains, all employing five active elements, is shown. The type of active element is indicated for each trace. All designs are constant-K except for the variable design with the highest gain.

five cascode elements. Another design, with seven cascode elements, has been carried out and indicates that 10 dB of gain from 2 to 30 GHz is achievable.

V. Fabrication

To the best knowledge of the authors, this circuit is the first report of a MMIC to be fabricated on organometallic vapor phase epitaxial (OMVPE) GaAs. Three epilayers consisting of a 1.0-micron undoped buffer layer followed by 1800 Å of active and 1200 Å of ohmic contact layer were grown on semi-insulating substrate. Doping of the active and contact layers was $5 \times 10^{17}/\text{cm}^3$ and $5 \times 10^{18}/\text{cm}^3$, respectively. FET's fabricated on OMVPE and MBE GaAs showed little or no difference in dc or RF performance. A distinct advantage was observed in using epi material as opposed to ion-implanted material, in that OMVPE FET's exhibited reduced g_m compression. In fact, the uniformity of the epilayer doping made FET and circuit performance less sensitive to gate recess etch depth. In applications which require low current consumption or noise figure, I_{dss} can be tailored to a reduced value by simply etching deeper. This is supported by the fact that the high gain result described in this paper was achieved with 150 mA of total drain current.

Fabrication of the cascode distributed amplifier included the following process steps in the sequence shown:

1) mesa etch for electrical isolation,
2) ohmic metal deposition and patterning,
3) SiO_2 deposition (sputtered) for MIM capacitors,
4) gate exposure (e-beam), etch, and metallization,
5) airbridge and plate,
6) backside via etch and plating.

A key feature of the fabrication process was the utilization of low-temperature sputtered oxide for MIM capacitor dielectric. Fabrication of the circuit would not have been possible otherwise, since it was found that other high-temperature oxide coating techniques caused a peculiar surface degradation and subsequent gate etch problems. The sputtered SiO_2 was patterned using the lift-off technique.

Quarter-micron gates of over 90 percent optical yield per wafer were fabricated by exposing a single layer of PMMA with a computer-controlled SEM. The SEM was fully automated, and software was written to provide step-and-repeat exposing as well as automatic alignment and focusing. Exposed alignment marks on individual FET's are still visible, as seen in Fig. 5. Reduction in gate metallization breaks was markedly improved after it was discovered that tweezer damage to the PMMA during processing caused particulate obscuration of the gate opening during metallization. This problem was particularly acute, since an individual gate yield of 90 percent translates to a circuit yield of only 35 percent according to the formula

$$y = \%\ \text{gate yield}/100$$

$$\%\ \text{circuit yield} = 100 \cdot y^N$$

where N is the number of FET's in the circuit.

Good grounding at critical points within the amplifier is crucial for nonoscillatory performance of the cascode design. Backside vias with dimension 40 μm$\times$80 μm were incorporated on one wafer and are indicated by white boxes in Fig. 4. Good RF grounding of the common-gate FET's is crucial and is achieved with the row of five vias contacting the bottom plate of the large-arched-area MIM capacitor shown in the figure. Reactive ion etching was used to etch 4-mil-deep holes, which were then plated with a pulse-plating technique. Because wafer thinning to 4 mils is first performed, the wafers are prone to cracking, which further reduces the number of working circuits.

VI. Testing and Results

Biasing of the cascode distributed amplifier is identical to the common-source FET amplifier except that an additional bias on the gate of the common-gate FET (as shown in Fig. 1b) is required. This bias is applied to one of the two tabs which contact the top plate of the large-arched-area common-gate ground capacitor shown in Fig. 4. By varying this additional bias, the gain of the circuit is adjustable and thus provides an added feature of automatic gain control. A dc measurement of an amplifier is displayed in Fig. 7, yielding a total g_m of 250 mmhos for 940 μm of gate periphery. Note the extremely low output conductance, which is characteristic of the cascode design.

Fig. 4 shows that the amplifier is compatible with the new RF wafer-probe measurement technique. RF measurements from 2 to 20 GHz were taken using this technique, and Fig. 8 displays results of over 10 dB from 2 to 18 GHz. This is the highest reported gain for a single-stage distributed amplifier at this bandwidth. Return loss is greater than 10 dB throughout the band. The high-gain region at the low end of the band is due to gate and drain line terminations of 80 Ω instead of 50 Ω. This is seen quantitatively with the dc gain expression for distributed amplifiers

$$|S_{21}|^2 = \frac{g_m^2 R_L^2}{4}$$

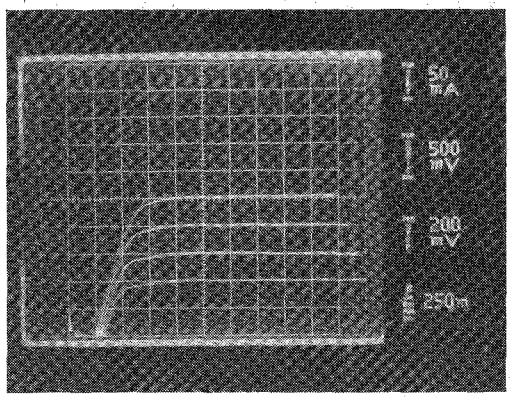

Fig. 7. dc $I_{ds}-V_{ds}$ characteristic for cascode distributed amplifier. The total g_m is 250 mmhos. Note the extremely low output conductance.

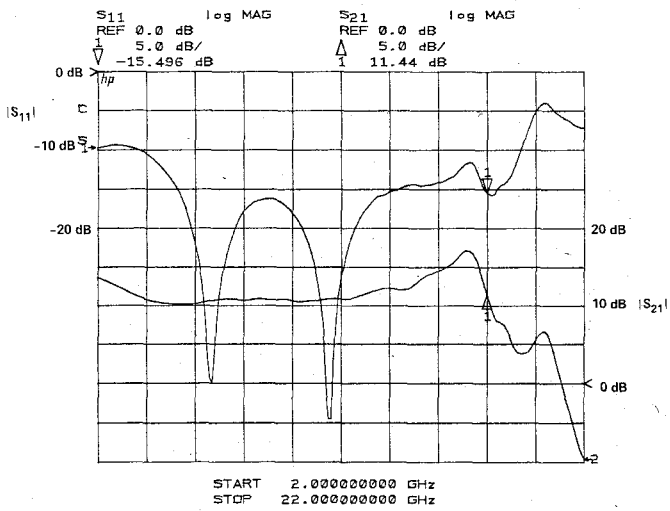

Fig. 8. Cascode distributed amplifier gain and return loss from 2 to 22 GHz.

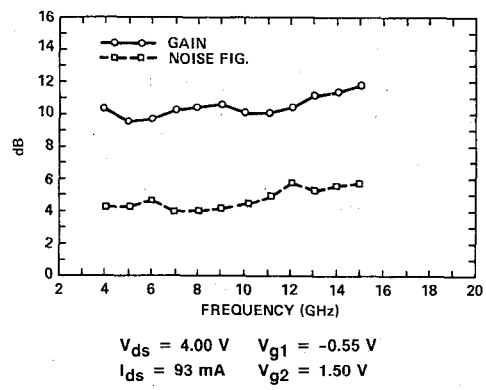

Fig. 9. Minimum noise figure and associated gain. Bias is adjusted for minimum noise. The minimum noise figure of 4 dB at 7 GHz has an associated gain of 10 dB.

where R_L is the termination resistance. The high-gain region of the upper bandedge is due to poor RF grounding of the common-gate FET. Poor RF grounding of these gates can lead to oscillations at the upper bandedge. Computer simulation indicates that one these problems are overcome by a reduction in termination resistance and backside vias, flat gain response of 12 dB$\pm$0.25 dB is achievable. In fact, a few circuits fabricated with backside

vias had stable upper bandedge response, but other problems thwarted perfect results. Both corrections have been incorporated in circuits under fabrication at the time of this writing.

Noise figure and associated gain were measured from 4 to 15 GHz using the same RF wafer probe station, and these results, displayed in Fig. 9, record a noise figure of 4 dB and associated gain of over 10 dB at 7 GHz. The noise figure above 15 GHz is markedly degraded, but is attributed to the aforementioned grounding problems only. The low value of I_{dss} is responsible for simultaneous high gain and low noise figure. It must be emphasized that the lower noise figures are attributable to the low drain current and use of quarter-micron gate lengths and not to the cascode configuration [5], [8].

VII. Conclusions

The results presented in this paper substantiate the hypothesis that reduction in gate and drain line loss will result in high-gain distributed amplifiers. It has been shown that a reduction in loss is possible by replacing the longer gate length common-source FET with the quarter-micron cascode element. A reduction in loss allows for the incorporation of additional FET periphery, thereby raising the overall gain level. Furthermore, by using epitaxial material with uniformly doped layers, high-gain performance is possible with low I_{dss}. The resulting low drain current combined with quarter-micron gate lengths reduces the noise figure of the amplifier.

Acknowledgment

The authors would like to acknowledge the excellent help of C. Nishimoto in ironing out details of the e-beam process. Additionally, we thank M. Day for process development.

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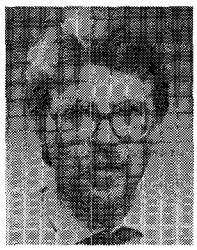

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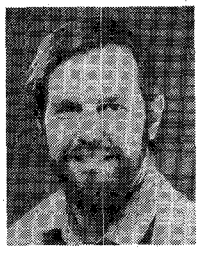

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